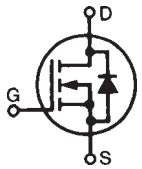
IXYS

High Voltage MOSFET

IXTA 1N100
IXTP 1N100

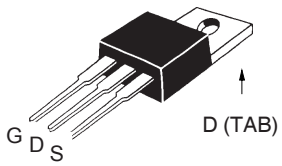
V_{DSS} = 1000 V
I_{D25} = 1.5 A
$R_{DS(on)}$ = 11 Ω

N-Channel Enhancement Mode
Avalanche Energy Rated

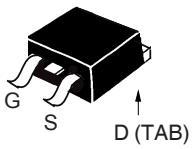


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	1000	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	1000	V
V_{GS}	Continuous	±30	V
V_{GSM}	Transient	±40	V
I_{D25}	T_C = 25°C	1.5	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	6	A
I_{AR}		1.5	A
E_{AR}	T_C = 25°C	6	mJ
E_{AS}	T_C = 25°C	200	mJ
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 18 Ω	3	V/ns
P_D	T_C = 25°C	54	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		4	g
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	°C

TO-220AB (IXTP)



TO-263 AA (IXTA)



G = Gate, D = Drain,
S = Source, TAB = Drain

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 μA	1000			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 25 μA	2.5		4.5	V
I_{GSS}	V_{GS} = ±30 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0 V, T_J = 25°C			25	μA
	$V_{DS} = V_{DSS}$, V_{GS} = 0 V, T_J = 125°C			500	μA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 1.0A, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			11	Ω

Features

- International standard packages
- High voltage, Low $R_{DS\ (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Fast switching times

Applications

- Switch-mode and resonant-mode power supplies
- Flyback inverters
- DC choppers
- High frequency matching

Advantages

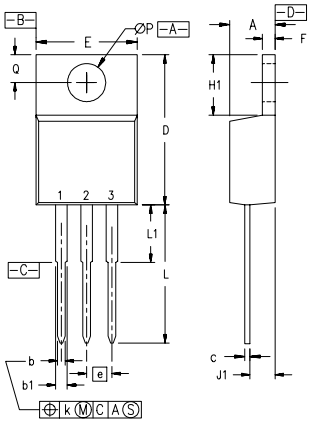
- Space savings
- High power density

Symbol	Test Conditions (T$_J$ = 25°C, unless otherwise specified)	Characteristic Values min.	typ.	max.	
g_{fs}	V_{DS} = 20 V; I_D = 1.0A, pulse test	0.8	1.5		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		400		pF
C_{oss}			37		pF
C_{rss}			13		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 1A R_G = 18Ω, (External)		18		ns
t_r			19		ns
$t_{d(off)}$			20		ns
t_f			18		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 • V_{DSS}, I_D = 1A		14.5		nC
Q_{gs}			3.0		nC
Q_{gd}			7.5		nC
R_{thJC}				2.3	K/W
R_{thCK}	(IXTP)		0.50		K/W

Source-Drain Diode

Symbol	Test Conditions (T$_J$ = 25°C, unless otherwise specified)	Characteristic Values min.	typ.	max.	
I_S	V_{GS} = 0 V			1.5	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			6	A
V_{SD}	$I_F = I_S$, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			1.8	V
t_{rr}	$I_F = I_S$, -di/dt = 100 A/µs, V_R = 100 V		710		ns

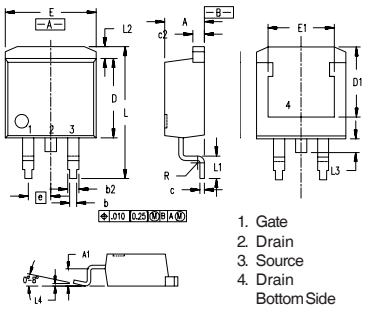
TO-220 AD Dimensions



Pins: 1 - Gate 2 - Drain
3 - Source 4 - Drain
Bottom Side

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
c	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
e	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
ØP	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

TO-263 AA Outline



1. Gate
2. Drain
3. Source
4. Drain
Bottom Side

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	4.06	4.83	.160	.190
A1	2.03	2.79	.080	.110
b	0.51	0.99	.020	.039
b2	1.14	1.40	.045	.055
c	0.46	0.74	.018	.029
c2	1.14	1.40	.045	.055
D	8.64	9.65	.340	.380
D1	7.11	8.13	.280	.320
E	9.65	10.29	.380	.405
E1	6.86	8.13	.270	.320
e	2.54	BSC	.100	BSC
L	14.61	15.88	.575	.625
L1	2.29	2.79	.090	.110
L2	1.02	1.40	.040	.055
L3	1.27	1.78	.050	.070
L4	0	0.38	0	.015
R	0.46	0.74	.018	.029

Fig. 1. Output Characteristics @ 25ºC

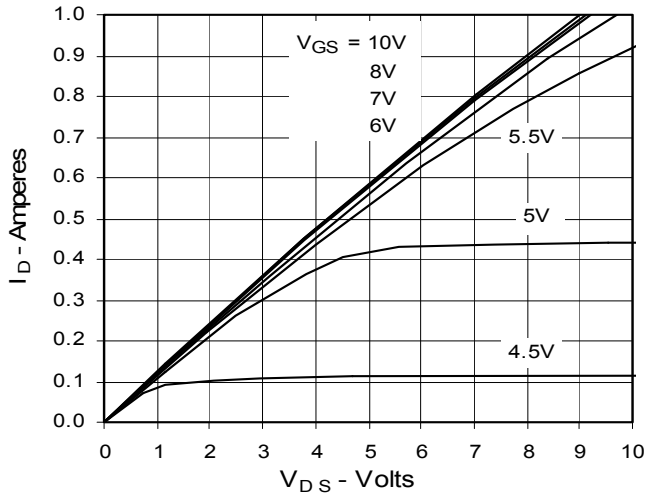


Fig. 2. Extended Output Characteristics @ 25ºC

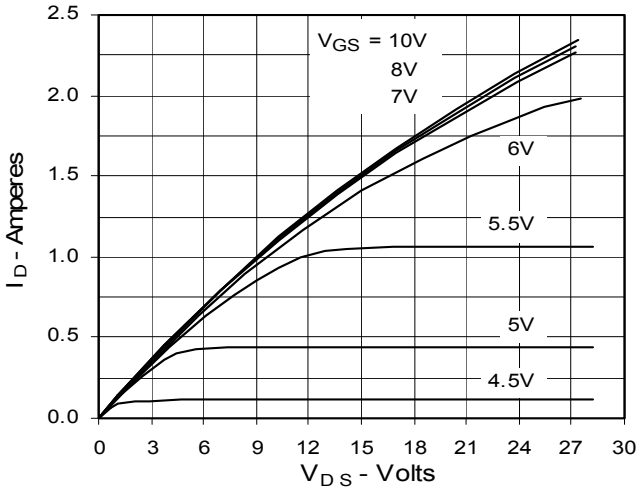


Fig. 3. Output Characteristics @ 125ºC

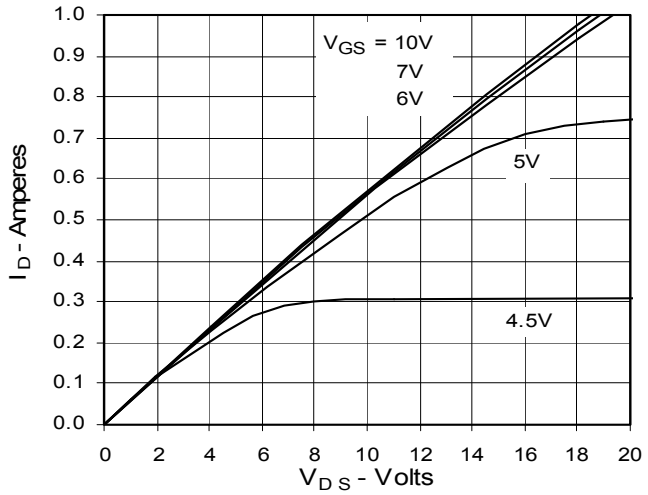


Fig. 4. Normalized $R_{DS(on)}$ vs. Junction Temperature

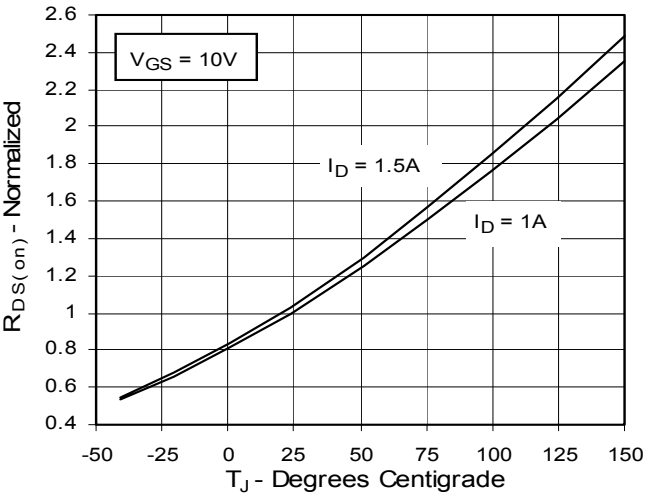


Fig. 5. Normalized $R_{DS(on)}$ vs. I_D

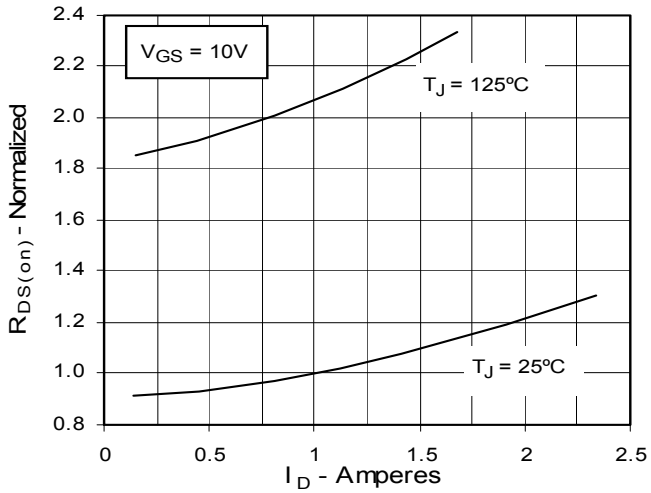


Fig. 6. Drain Current vs. Case Temperature

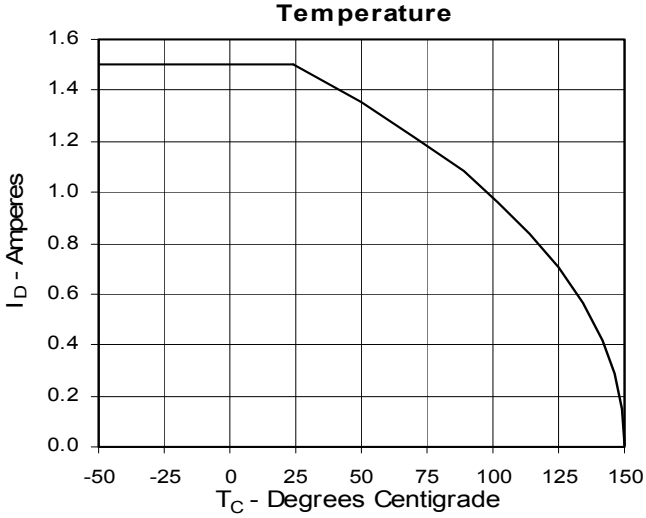


Fig. 7. Input Admittance

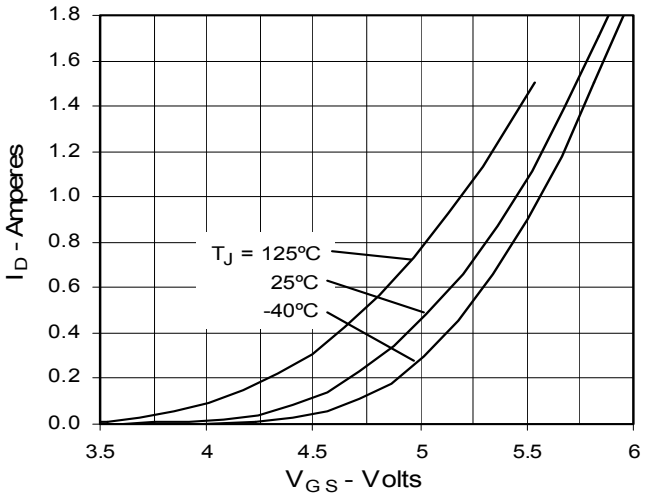


Fig. 8. Transconductance

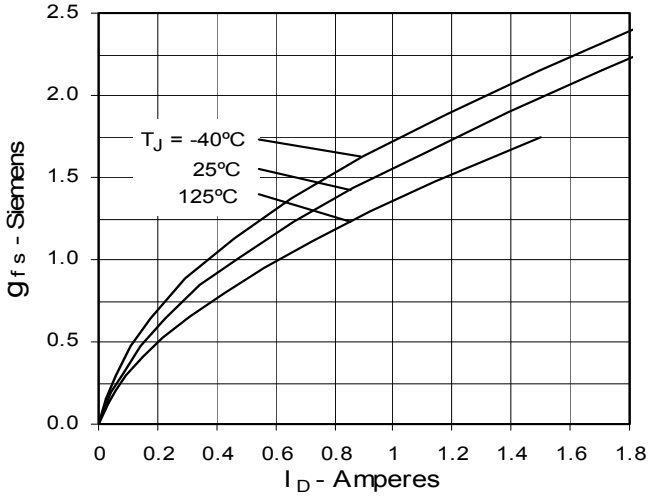


Fig. 9. Source Current vs. Source-To-Drain Voltage

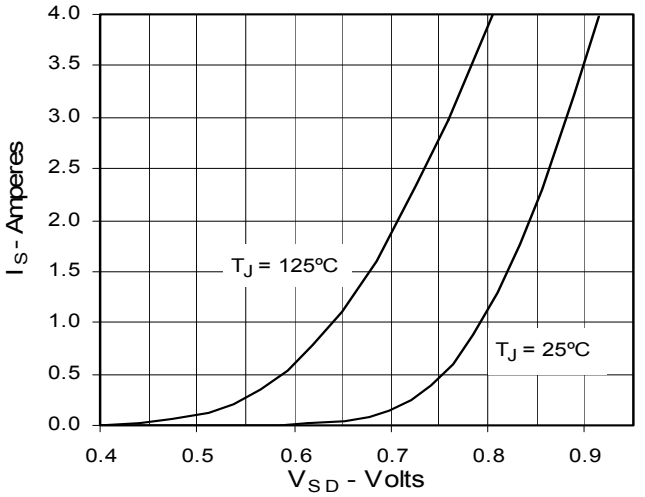


Fig. 10. Gate Charge

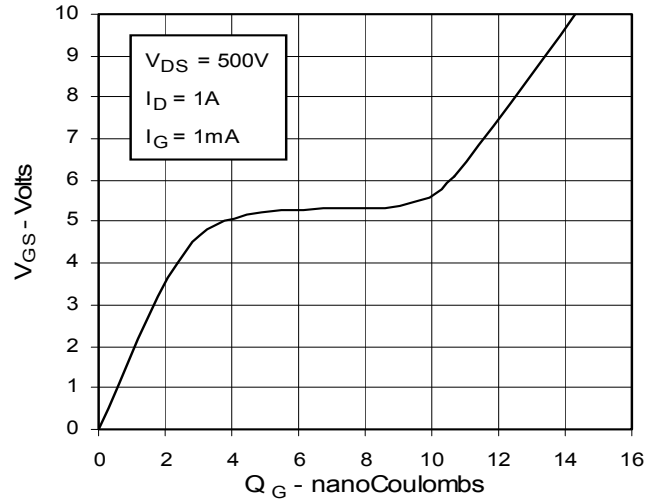


Fig. 11. Capacitance

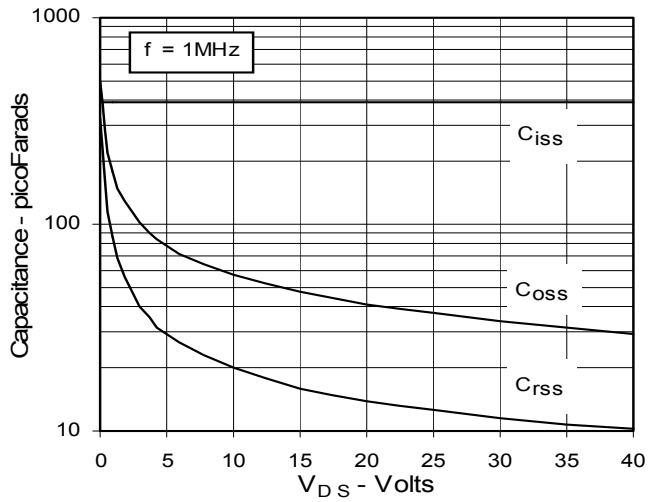


Fig. 13. Maximum Transient Thermal Resistance